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Reg. No. : .....

Name : .....

# Third Semester B.Tech. Degree Examination, October 2016
## (2013 Scheme)
## 13.305 : DIGITAL SYSTEM DESIGN (FR)

Time : 3 Hours Max. Marks : 100



PART – A

Answer **all** questions. **Each** question carries **2** marks.

1. Express the Boolean function $F = A' + B'C$ as a sum of minterms.
2. Design a Half Adder Circuit.
3. Simplify the following Boolean expression using K-map.

   $F = x'yz + x'yz' + xy'z' + xy'z$.
4. Draw the logic diagram of D-Flip-flop with NAND gates. Briefly discuss the operation of the circuit.
5. Implement $F(A, B, C) = \sum(1, 3, 5, 7)$ with a Multiplexer.
6. What is meant by loading a register ? Explain.
7. Differentiate between synchronous and asynchronous counters.
8. Draw the timing diagram for BCD Counter.
9. How the divide overflow problem can be avoided ?
10. Differentiate between restoring and non-restoring division.

P.T.O.

## PART – B

Answer **one full** question from **each** Module. **Each** question carries **20** marks.

### Module – I

11. a) The following Boolean expression BE + B'DE' is a simplified version of the expression A'BE + BCDE + BC'D'E + A'B'DE' + B'C'DE'. Are there any don't care conditions ? If exists, what are they ?

    b) Obtain the simplified form of the given expression as a Sum of Products $F(A,B,C,D) = A'B'C'D' + AC'D' + B'CD' + A'BCD + BC'D$.

12. a) Simplify the following Boolean expression by using Tabulation Method.

    $F = \sum(0, 1, 2, 8, 10, 11, 14, 15)$

    b) Implement a full subtractor with 2 half subtractors and an OR Gate.

### Module – II

13. a) Design a combinational circuit that converts a Decimal digit from 8, 4, – 2, – 1 code to BCD.

    b) Design a Carry Look Ahead Adder Circuit.

14. a) Discuss the working of a clocked JK Flip-flop.

    b) Is it possible for a decoder to function as a Demultiplexer ? If yes, explain how ?

### Module – III

15. a) Discuss the working of BCD Ripple Counter. **15**

    b) What is meant by memory decoding ? Explain. **5**

16. a) Design a BCD to Gray code converter.

    b) Design a 2 × 4 Decoder in HDL.

### Module – IV

17. a) Explain Booth's Multiplication Algorithm with an example.

    b) Give an algorithm for the multiplication of two BCD numbers.

18. a) Discuss an algorithm for the addition of 2 Floating point numbers.

    b) Discuss the working of an Array Multiplier.

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